Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

1. (Currently amended) A method for fabricating [[a]] capacitors, vias, and conductors in an interlayer dielectric (ILD) comprising:

forming a plurality via and overlying trench in the ILD;

depositing a first conductive barrier layer so as to line the vias and trenches;

depositing a dielectric layer over the first conductive barrier layer;

depositing a second conductive barrier layer over the dielectric layer;

covering at least some of the vias and overlying trenches;

removing the second conductive barrier layer and dielectric layer from the vias and overlying trenches not covered;

filling the vias and trenches with a conductive material that includes copper ~~over the second conductive barrier layer~~; and

polishing back the conductive material so as to expose the ILD adjacent to the trench.

2. (Currently amended) The method defined by claim 1 wherein ~~the~~ at least one of the first and second barrier layers comprises tantalum.

3. (Currently amended) The method defined by claim 1 wherein the dielectric layer is selected from the group consisting of silicon nitride, titanium oxide, tantalum penta oxide, ~~or~~ and barium-strontium-titanate.

4. (Currently amended) The method defined by claim 1 including the deposition of [[a]] conductive electrode layers between the first conductive barrier layer and the dielectric layer and between the dielectric layer and the second conductive barrier layer.

5. (Currently amended) The method defined by claim 4 wherein the electrode layers comprise a material selected from the group consisting of ruthenium ~~or~~ and iridium.

6. (Currently amended) The method defined by claim 1 wherein the vias exposes ~~an~~ underlying conductors.

Claims 7-12 (Cancelled)

13. (Original) In a dual damascene process an improvement comprising:

lining ~~selective~~ vias and trenches in an ILD with a first and second conductive barrier layer having a dielectric disposed therebetween; ~~prior to a copper layer formation; and~~

~~polishing the copper layer~~ removing the second barrier layer and dielectric from selected ones of the vias and trenches; and

forming a conductive material in the vias and trenches.

14. (Currently amended) The process defined by claim 13 wherein the dielectric is selected from the group consisting of silicon nitride, titanium oxide, ~~or~~ and barium-strontium-titanate.

15. (Currently amended) The process defined by claim 13 wherein the first and second conductive barrier layer comprises tantalum

16. (Currently amended) The process defined by claim 13 wherein electrode layers are used between the barrier layers and the ~~copper layer~~ conductive material.

17. (Original) The process defined by claim 13 where the first barrier layer is in contact with an underlying conductor.

18. (Currently amended) A method for fabricating capacitors and via interconnects in an interlayer dielectric (ILD) comprising:

forming a plurality of vias and overlying trenches;

forming a capacitor structure which includes a dielectric layer on the ILD and within the vias and trenches;

removing ~~a~~ the dielectric layer from the capacitor structure from selected vias and trenches, leaving a first conductive barrier layer in the selected vias and trenches;

forming a conductive material in the vias and trenches such that some of the vias and trenches have capacitors and others have interconnects.

19. (Currently amended) The method defined by claim 18 ~~including the steps of~~ wherein forming a conductive material comprises forming a copper layer and polishing the copper layer after ~~the step of~~ removing the dielectric layer from the capacitor structures in the selected vias and trenches.

20. (Original) The method defined by claim 19 wherein the polishing step includes removing all material on the ILD between the trenches.

21. (Currently amended) The method defined by claim 19 wherein the step of forming the capacitor structure comprises the steps of forming ~~a~~ the first conductive barrier layer, forming ~~a~~ the dielectric layer and forming a second conductive barrier layer.

22. (Currently amended) The method defined by 21 including ~~the steps of~~ adding electrode layers between the barrier layers and the dielectric layer.

23. (Withdrawn) A capacitor comprising a first and second conductive layer separated by a dielectric defining a first stepped sidewall, a mirror image second stepped sidewall facing the first sidewall and a base disposed between the lower ends of the first and second sidewalls.

24. (Withdrawn) The capacitor defined by claim 23 wherein the first and second conductive layers comprise a metal which acts as a barrier layer to copper.

25. (Withdrawn) The method defined by claim 24 including additional metal layers disposed between the first conductive layer and the dielectric and the second conductive layer and the dielectric.

26. (Withdrawn) The capacitor defined by claim 23 wherein the dielectric is selected from the group consisting of silicon nitride, titanium oxide, tantalum penta oxide, or barium-strontium-titanate.